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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,777	MARR ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE, Extension of Time, and Amendment as received on 8/5/2005.

Specification

3. The disclosure is objected to because of the following informalities: On page, 11, paragraph [0027], replace "370" with --365--.

Appropriate correction is required.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "195" has been used to designate both the memory and thread 1 in Fig.1. According to paragraph [0016] of the specification, it appears that thread 1 should be assigned number "196". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Paragraph [0017] of the specification refers to number "170" in Fig.1. However, number "170" is not found in Fig.1.

Paragraph [0018] of the specification refers to number "180" in Fig.1. However, number "180" is not found in Fig.1.

Paragraph [0025] of the specification refers to number "340" in Fig.3a. However, number "340" is not found in Fig.3a.

Paragraph [0031] of the specification refers to numbers "1100, 1110, 1120, 1140, 1150, and 1160" in Fig.5. However, these numbers are not found in Fig.5.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Maintained Rejections

6. Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 24-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, the examiner has been unable to locate any particular structure(s) in the specification that perform(s) the relinquishing and/or re-partitioning of resources. And, one of ordinary skill in the art would not necessarily know what type of structure is capable of relinquishing/re-partitioning resources. Since applicant is claiming means for performing such functions, structures corresponding to those functions must be described. See MPEP 2163, part 3(a). If applicant believes that a structure is disclosed which performs the relinquishing and re-partitioning functions, then it is asked that applicant point out the structure in the specification.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 24-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 24 includes a means for relinquishing resources and a means for re-partitioning resources. It appears as though applicant discloses the functions of relinquishing and re-partitioning but discloses no express, implied or inherent disclosure of hardware or a combination of hardware and software that performs the functions. Therefore, the application has not disclosed any "structure" which corresponds to the claimed means. If applicant feels that a structure has been disclosed, applicant must describe at least one specific structure or material that corresponds to the claimed means in question, and to identify the precise location or locations in the specification where a description of at least one embodiment of that claimed means can be found. See MPEP 2106, section V, part A2.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-26 rejected under 35 U.S.C. 102(e) as being anticipated by Kalafatis et al., U.S. Patent Number 6,535,905 (as applied in the previous Office Action and herein referred to as Kalafatis).

14. Referring to claims 1 and 18 Kalafatis has taught a processor comprising: a memory to store a plurality of program threads (Kalafatis figure 3 number 106);

a plurality of thread partitionable resources that are each partitionable between a plurality of threads (Kalafatis figure 4; note that any combination of components including one of components 106, 62, 103, and retirement logic is a partitionable resource; column 13 lines 32-38);

a processor coupled to said memory; See Fig.4, component 44.

logic to receive a program instruction from a first thread of said plurality of threads, and in response to said program instruction to cause the processor to suspend execution of the first thread and to relinquish portions of said plurality of thread partitionable resources associated with the first thread for use by other ones of said plurality of threads. See Kalafatis figure 14 figure 8 column 10 lines 25-39, column 18 lines 62-column 19 line 36; switching takes place between threads when a branch instruction occurs, and also at an instruction, or inserted flow, is inserted in the instruction sequence. For example, components 103, 72, and 70, of Fig.4, make up an overall partitionable resource. When thread 0 is active, thread 0 instructions are sent from the corresponding IQ partition to the execution unit. When thread 0 is suspended, for whatever reason, the execution portion of the resource is relinquished so that it may be used by thread 1 (or another thread if one exists).

15. Referring to claim 2 Kalafatis has taught wherein the program instruction is a suspend instruction which consists of a suspend opcode which explicitly directs the processor to suspend execution of the first thread and to relinquish portions of said plurality of thread partitionable resources associated with the first thread for use by other ones of said plurality of threads (Kalafatis figure 14, column 18 lines 62-column 19 line 36; switching takes place between threads when an instruction, or inserted flow, is inserted in the instruction sequence).

16. Referring to claim 3 Kalafatis has taught wherein said logic is to cause the processor to suspend the first thread for a selected amount of time (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63).

17. Referring to claim 4 Kalafatis has taught wherein said selected amount of time is a fixed amount of time (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63; the number is predetermined).

18. Referring to claims 5 and 19 Kalafatis has taught wherein said processor is to execute instructions from a second thread while said first thread is suspended (Kalafatis column 2 lines 3-12, column 4 lines 10-49).

19. Referring to claims 6 and 20 Kalafatis has taught wherein said selected amount of time is programmable by at least one technique chosen from a set consisting of:

providing an operand in conjunction with the program instruction; blowing fuses to set the selected amount; setting the selected amount in microcode (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-column 14 line 6; since the number is predetermined, it is programmable by the control register bus).

20. Referring to claims 7 and 21 Kalafatis has taught wherein said plurality of thread partitionable resources comprises: an instruction queue (Kalafatis figure 4 number 103); a register pool (Kalafatis column 13 lines 32-46).

21. Referring to claims 8 and 22 Kalafatis has taught further comprising: a plurality of shared resources, said plurality of shared resources comprising: a plurality of execution units (Kalafatis figure 4 number 70); a cache (Kalafatis figure 4 number 44); a scheduler (Kalafatis figure 4 number 72); a plurality of duplicated resources, said plurality of duplicated resources comprising: a plurality of processor state variables; an instruction pointer; register renaming logic (Kalafatis figure 4 number 76/78, 100).

22. Referring to claims 9 and 23 Kalafatis has taught wherein said plurality of thread partitionable resources further comprises: a plurality of re-order buffers; a plurality of store buffer entries (Kalafatis column 13 lines 32-46).

23. Referring to claim 10 Kalafatis has taught wherein said logic is further to cause the processor to resume execution of said first thread in response to an event (Kalafatis column 8 lines 5-36).

24. Referring to claim 11 Kalafatis has taught wherein said logic is further to cause the processor to ignore events until said selected amount of time has elapsed (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63; the number is predetermined).

25. Referring to claim 12 Kalafatis has taught wherein said processor is embodied in digital format on a computer readable medium (Kalafatis column 1 line 5-column 2 line 15).

26. Referring to claims 13 and 24 Kalafatis has taught a method comprising:

receiving a first opcode in a first thread of execution;

suspending said first thread for a selected amount of time in response to said first opcode;

relinquishing a plurality of thread partitionable resources in response to said first opcode (Kalafatis figure 14 figure 8 column 10 lines 25-39, column 18 lines 62-column 19 line 36; switching takes place between threads when a branch instruction occurs (i.e., branch opcode is detected), and also at an instruction, or inserted flow, is inserted in the instruction sequence). For example, components 103, 72, and 70, of Fig.4, make up an overall partitionable resource. When thread 0 is active, thread 0 instructions are sent from the corresponding IQ partition to the execution unit. When thread 0 is suspended, for whatever reason, the execution portion of the resource is relinquished so that it may be used by thread 1 (or another thread if one exists).

re-partitioning said plurality of resources after a selected amount of time (Kalafatis column 10 lines 62-column 11 line 19, column 7 lines 8-35). For example, again taking components 103, 72, and 70, of Fig.4, as a resource, it can be seen that when thread 0 is active, then the resource is partitioned such that the thread-0 portion of the IQ, the scheduler, and the execution unit, are all assigned to operating on thread 0, whereas the thread-1 portion of the IQ is assigned to thread 1. When thread 1 becomes active, the resource is repartitioned such that the thread-1 portion of the IQ, the scheduler, and the execution unit, are all assigned to operating on thread 1, whereas the thread-0 portion of the IQ is assigned to thread 0. Then, ultimately, when thread 0 becomes active again, the resource is repartitioned such that the thread-0 portion of the IQ, the scheduler, and the

execution unit, are all assigned to operating on thread 0, whereas the thread-1 portion of the IQ is assigned to thread 1.

27. Referring to claim 14 Kalafatis has taught wherein relinquishing comprises: annealing the plurality of thread partitionable resources to become larger structures usable by fewer threads (Kalafatis column 7 lines 8-35, figure 2).

28. Referring to claims 15 and 26 Kalafatis has taught wherein relinquishing said plurality of thread partitionable resources comprises: relinquishing a partition of an instruction queue(Kalafatis figure 4 number 103) ; relinquishing a plurality of registers from a register pool (a register pool (Kalafatis column 13 lines 32-46).

29. Referring to claim 16 Kalafatis has taught wherein relinquishing said plurality of thread partitionable resources further comprises: relinquishing a plurality of store buffer entries; relinquishing a plurality of re-order buffer entries (Kalafatis column 13 lines 32-46).

Referring to claim 17 Kalafatis has taught wherein said selected amount of time is programmable by at least one technique chosen from a set consisting of:

providing an operand in conjunction with the first opcode;

blowing fuses to set the selected amount of time;

programming the selected amount of time in a storage location in advance of decoding the program instruction;

setting the selected amount of time in microcode (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-column 14 line 6; since the number is predetermined, it is programmable by the control register bus).

30. Referring to claim 25 Kalafatis has wherein said first instruction is a macro-instruction from a user-executable program (Kalafatis column 3 line 45-column 4 line 7).

Response to Arguments

31. Applicant's arguments filed on August 5, 2005, have been fully considered but they are not persuasive.

32. Throughout the remarks, applicant's argument is that Kalafatis does not teach relinquishing and repartitioning a plurality of thread partitionable resources (or portions thereof).

33. These arguments are not found persuasive for the following reasons:

a) As described above, components 103, 72, and 70, of Fig.4, make up an overall partitionable resource. When thread 0 is active, thread 0 instructions are sent from the corresponding IQ partition to the execution unit via the scheduler. When thread 0 is suspended, for whatever reason, the execution unit portion 70 of the resource is relinquished so that it may be used to execute thread 1 (or another thread if one exists). Hence, it can be seen that portions of resources are relinquished,

b) In addition, again taking components 103, 72, and 70, of Fig.4, as a resource, it can be seen that when thread 0 is active, then the resource is partitioned such that the thread-0 portion of the IQ, the scheduler, and the execution unit are all assigned to thread 0, whereas the thread-1 portion of the IQ is assigned to thread 1. When thread 1 becomes active, the resource is repartitioned such that the thread-1 portion of the IQ, the scheduler, and the execution unit are all assigned to thread 1, whereas the thread-0 portion of the IQ is assigned to thread 0. Then, ultimately, when thread 0 becomes active again, the resource is repartitioned such that the

thread-0 portion of the IQ, the scheduler, and the execution unit are all assigned to operating on thread 0, whereas the thread-1 portion of the IQ is assigned to thread 1. Hence, it can be seen that repartitioning of resources occurs.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Joy et al., U.S. Patent No. 6,341,347, has taught thread switch logic in a system which partitions resources such as data cache for multiple threads. The partitioning may be disabled for certain types of threads.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
September 21, 2005

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